Amendments to the Specification:

Please move the Related applications: paragraph from page 3 to page 2 before the Background of Invention. Change the title of the Related applications: paragraph to Cross-Reference to Related Applications:.

Please replace the paragraph under Cross-Reference to Related Applications: on page 2, with the following rewritten paragraph:

Patent applications entitled, "APPARATUS AND METHOD FOR MULTI-CHANNEL COMMUNICATIONS SYSTEM" serial number 09/695,647 and "APPARATUS AND METHODS FOR MULTI-CHANNEL RECEIVER" serial number 09/695,536, both filed on October 24, 2000, having the same inventor and assigned to the same assignee as this application are hereby incorporated by reference.

Please replace the paragraph beginning on page 2, line 24 with the following rewritten paragraph:

Centralized headend and distributed headend communications systems are known and discussed, for example, in U.S. Patent 5,841,468 ~~5,41,468~~ entitled, SYSTEM AND METHOD FOR ROUTING DATA MESSAGES THROUGH A CABLE TRANSMISSION SYSTEM, issued to Wright, U.S. Patent 6,100,883, entitled, HOME INTERFACE CONTROLLER FOR PROVIDING INTERACTIVE CABLE TELEVISION, issued to Hoarty, and U.S. Patent 5,999,970, entitled, ACCESS SYSTEM AND METHOD FOR PROVIDING INTERACTIVE ACCESS TO AN INFORMATION SOURCE THROUGH A TELEVISION DISTRIBUTION SYSTEM, issued to Krisbergh et al., all of which are herby incorporated by reference.

Please replace the paragraph beginning on page 7, line 11 with the following rewritten paragraph:

The conceptual block diagram of Figure 1 illustrates a communication system 100 in accordance with the principles of the present invention that employs digitally modulated signals operating in a band of frequencies that is divided into two or more non-overlapping channels, with each channel occupying no more than a predetermined maximum frequency band. In an illustrative embodiment, the system 100 includes a transmitter 102 and a receiver system 104. The transmitter 102 transmits digitally modulated signals operating in a band of frequencies that is divided into two or more non-overlapping channels, with each channel occupying no more than a predetermined maximum frequency band. The receiver system 104 may include an analog to digital converter (ADC) 106, a front end processor 108 and a back end processor, or receiver 110. The front end processor 108 may be configured to receive a data stream that represents the entire frequency band sampled at a rate that is at least twice the highest frequency within the frequency band. In an illustrative embodiment, a single ADC may be employed to sample the entire frequency band at this rate.

Please replace the paragraph beginning on page 8, line 6 with the following rewritten paragraph:

The digitally modulated signals employed by a communications system in accordance with the principles of the present invention may occupy a band of frequencies that stretch from a lower frequency bound A to an upper frequency bound B, as illustrated in the frequency diagram of Figure 2A. In accordance with the principles of the present invention, this frequency band

may be divided into two or more non-overlapping channels, as illustrated in the frequency diagram of Figure 2B. In a data over cable service interface specification (DOCSIS) [[-]] compliant embodiment, the lower A and upper B frequency bounds are 5 and 42 Mhz, respectively and that band may be divided into non-overlapping channels of .2 MHz,_.4 MHz,_.8 MHz,_1.6 MHz, or 3.2MHz. The center frequencies of these channels may be selected in a manner that avoids interference and may be chosen with complete flexibility, so long as the resulting channels are non-overlapping as generally illustrated in the frequency diagram of Figure 2C. For example, in order to avoid interference at 7MHz in a DOCSIS system, a .2MHz channel may be centered at 6.8 MHz, and a .8MHz channel may be centered at 7.6MHz, as illustrated in the frequency diagram of Figure 2D. In DOCSIS and other, non-DOCSIS compliant embodiments, a communications system in accordance with the principles of the present invention may employ a scheme whereby the frequency band from A to B organized into group channels G1, G2, etc., each of which includes one or more channels, ~~as~~ is illustrated in the frequency diagram of Figure 2E. In one aspect of the invention, the communications system 100 may be a cable television system, as illustrated in the conceptual block diagram of Figure ~~2~~3, that provides for upstream communications through one or more coaxial cables 300 from subscribers 302 to a "headend" 304 that includes a receiver system 104. Each of the subscribers 302 transmits information to the headend 304 using a transmitter (not shown) such as the transmitter 102 of Figure 1.

Please replace the paragraph beginning in page 9, line 1 with the following replacement paragraph:

In an illustrative embodiment, ~~the~~ system ~~100~~ 310 is a DOCSIS compliant system in which each of the transmitters, as previously described, may transmit in assigned channels within the upstream frequency band from approximately 5 to 42 MHz. This band may be divided into channels .2 MHz,.4 MHz,.8 MHz,1.6 MHz, or 3.2MHz wide. In a DOCSIS compliant embodiment of the system 100, such as system 310 illustrated in Figure 3, there may be as many as 20,000 subscribers 302 serviced by a single headend 304. In addition to downstream signals provided by the headend to subscribers, which typically may fall within the 45 MHz to 860MHz band, the subscribers 302 may transmit digital information to the headend 304 and, although such information was once limited to such things as "pay per view" selections, more recently such information may include various forms of data communication in conjunction with the use of the Internet, or digitized voice traffic, for example. Each of the coaxial cables 300, in spite of a grounded shielding surface surrounding and coaxial with a center signal conductor, acts as an antenna that is capable of picking up electrical noise and interference and superimposing this unwanted signal on a desired signal. Each of numerous points of connection within the system (not shown) also permit the admission of noise and interference. In order to avoid such interference, subscribers may transmit information, on upstream channels selected to avoid such interference, as described in the discussion related to Figure 2D.

Please replace the paragraph beginning on page 9, line 19 with the following replacement paragraph:

Although the system 100 may be organized in a manner whereby a single headend may service tens of thousands of subscribers and adhere to the DOCSIS standard for upstream

communications, the system may also employ a distributed array of two or more "mini-headends" 400, 402, 404, as illustrated in the conceptual block diagram of Figure 4. In this illustrative embodiment, each mini-headend services N or fewer subscribers 406, where N is no more than 500. The mini-headends, 400, 402, and 404 may be located in remote locations and that form the boundary between coaxial and optical fiber communications, with coaxial ~~cable~~ cables 408 forming the links between subscribers an mini-headends and optical ~~fiber~~ fibers 410 forming the links between mini-headends and a headend 304. Whether the system employs a centralized headend, or distributed mini-headends, receiver systems at the point of conversion between coaxial cable and optical fiber transmission, whether that be within a centralized headend or within a plurality of distributed headends, includes a receiver system 104 which, as previously described, converts all channels within the upstream band to baseband, decimates each baseband channel signal to at least twice the symbol rate of the corresponding channel, and phase corrects, time corrects, and equalizes the data stream for all the constituent channels.

Please replace the paragraph beginning on page 10, line 6 with the following replacement paragraph:

With each mini-headend ~~302~~ 400, 402, and 404 serving a smaller group of subscribers, noise and interference on the cables 408 is substantially less than that on the cables 300 of Figure 3. Furthermore, the reduced number of subscribers per mini-headend may facilitate assigning a narrow frequency band to each subscriber which significantly increases Quality of Service. Since the mini-headends 400, etc. may well be positioned in remote neighborhood locations, the bulk, expense, and power consumption of each receiver system 104 should be minimized. As

previously described, the front end of the receiver system 104 reduces the number of ADCs required, in comparison with conventional receivers and, as will be described, may afford further savings in energy, bulk, and capital outlays.

Please replace the paragraph beginning on page 10, line 25 with the following replacement paragraph:

In accordance with the principles of the invention a front end processor 108 may be employed to accept a data stream 112 that represents the entire band of digitally modulated signals that comprise two or more non-overlapping channels, with each channel occupying no more than a predetermined maximum frequency sub-band, the entire band having been sampled at least twice the frequency of the highest frequency within the band. As depicted in the conceptual block diagram of Figure 5, the front end processor 108 includes a converter 500 that converts the component channels to baseband, and produces an output stream of baseband channel data for each channel CH1, CH2, ~~CHn~~CHN. The baseband channel data CH1, CH2, ~~CHn~~ CHN is passed to a decimator 502 which yields component baseband channel data sampled at least twice the symbol rate of each of the channels. As will be described in greater detail in the discussion related to the following Figures, the baseband conversion and decimation may take place in parallel, with, essentially, one step for each operation, or it may be performed in a more iterative fashion. In either case, the front end operates upon data for all the signals within the band of interest to produce an output baseband data stream 114 at twice the symbol rate of each of the band's constituent channels. The data stream 114 may be a single multiplexed, data stream or the data may be split into streams for each of the constituent channels.

Please replace the paragraph beginning on page 11, line 13 with the following replacement paragraph:

In the illustrative DOCSIS-compatible embodiment depicted in the conceptual block diagram of Figure 6 a front end processor 600 processes signals sampled at 102.4 mega-samples per second by demodulating and filtering all the channels within the upstream band in parallel. The front end processor 600 is a specific example of the previously described front end processor 108 and may be configured to operate on the entire upstream band converted to a single digital bit stream, such as may be accomplished by a single ADC sampling at the rate of at least twice the highest frequency in the band. Since, in a DOCSIS upstream signaling system the digitally modulated signals fall within non-overlapping upstream channels that are assigned within a 5 to 42 MHz band, the sample rate of 102.4 mega-samples per second in this illustrative embodiment is more than sufficient to meet the Nyquist criterion. Each non-overlapping channel has a bandwidth of approximately 3.2MHz, 1.6 MHz, .8 MHZ, .4 MHz, or .2 MHz and the upstream band may include any mix of such channels, centered on any frequency with the band, so long as the channels are non-overlapping. Each such channel carries digitally modulated information that may be in the form of pulse amplitude modulated (PAM), quadrature amplitude modulated (QAM), or other digitally modulated signaling schemes.

Please replace the paragraph beginning on page 12, line 1 with the following replacement paragraph:

The receiver front end processor 600 accepts this digitized channel information and converts each of the channels within the entire 5 to 42 MHz band to baseband, in parallel, and

may be used in conjunction with a receiver 110 such as described in the discussions related to Figures 12 and 13 to demodulate and decimate multi-channel signals such as DOCSIS upstream signals. A single ADC, such as ADC 106 of Figure 1 may convert the analog upstream signal to a digitized full-band data stream that is to be processed by the front end processor 600. That is, a single ADC may sample the entire 5 MHz – 42 MHz band to produce a digitized data stream for processing by the front end processor 600. The entire digital data stream is fed to each ~~of~~ down converters 602, 604, and 606, each of which is dedicated to one of the N channels within the upstream band. Each down converter includes a multiplier that multiplies the input digital bit stream by ~~$e^{j\omega_N n}$~~ $e^{j\omega_N n}$, where ω_N is the center frequency of a particular channel[[.]], to effect the conversion of each channels' data stream to a baseband signal, with the center frequency of the channel shifted to 0Hz. Each multiplier value is determined at the time channels are selected, as they might be to avoid interference.

Please replace the paragraph beginning on page 13, line 8 with the following replacement paragraph:

In the illustrative embodiment of Figure 7 a tree-structured front end processor 700 may be used in telecommunications applications where a broad frequency band is divided into groups of channels, hereinafter referred to as "group-channels" and the group channels may be further divided into individual channels, as illustrated in the frequency diagram of ~~Figures~~ Figure 8 where group channels GCH1, GCH2, GCH3, and GCHN are respectively divided into channels ~~ch1~~CH1, ~~ch2~~CH2, ~~ch3~~CH3; ~~ch4~~CH4; ~~ch5~~CH5, ~~ch6~~CH6, and ~~chn1~~CHN1, ~~chn2~~CHN2, ~~chn3~~CHN3, and ~~chn4~~CHN4. Each of the Group Channels occupies a predetermined frequency

band within a signaling band that extends from frequencies A to B and each group channel may be divided into channels of predetermined frequency widths.

Please replace the paragraph beginning on page 13, line 17 with the following replacement paragraph:

In accordance with the principles of the invention, the front end processor 700 may be configured in a tree-like topology to iteratively convert to baseband and decimate successively smaller portions of the entire band, yielding ~~a~~ I/Q data streams representing the component channels converted to baseband signals sampled at least twice the symbol rate of each of the channels. That is, the front end processor 700 may be configured to operate on the entire band from A to B (as represented in Figure 8) converted to a single digital bit stream, such as may be accomplished by a single ADC sampling at a rate of at least twice the highest frequency, B, in the band.

Please replace the paragraph beginning on page 14, line 14 with the following replacement paragraph:

At the digital input 754 the TDD 700 accepts a digital input stream of real data sampled at twice the frequency of the highest frequency of the group channel which comprises the N channels being down-converted and decimated. Unlike the front end processor described in the discussion related to Figure 6, which operates on signals having channels assigned with a great deal of flexibility , it is assumed in this illustrative embodiment that each of the channels operates at a predetermined, fixed carrier frequency. Such ~~as~~ a system might be particularly advantageous in a distributed hybrid fiber cable system, such as described in the discussion

related to Figure 4, since, in such a system the number of subscribers (substantially less than one thousand) contributing noise and interference to a particular cable link is drastically reduced in comparison to the number of subscribers (as many as twenty thousand) contributing noise and interference through cables to a conventional headend and, consequently, the motivation for flexibility in selecting upstream channels that avoid interference is greatly reduced. Such a fixed carrier frequency assignment system is compatible with the DOCSIS standard. Each of the down-converters ~~728~~ 702 through 726 multiplies the signal that it has received by a center frequency that, as illustrated in the frequency diagrams of Figures 9A to 9D shifts the segment of interest to baseband (that is, centers it at 0HZ). The subsequent decimation filters act as low pass filters to remove signals not of interest at a particular point in the TDD tree.

Please replace the paragraph beginning on page 15, line 3 with the following replacement paragraph:

For example, if the signal that emerges from decimation filter 728 includes three group channels, and the center group channel has a center frequency equal to $-\omega_a$, of 702, then only two follow-on decimation filters would actually be employed in the next tier of down-converters (704, 706, 708) and filters (730, 732, 734) with one down-converter dedicated to bring an upper group-channel to baseband, another dedicated to bring a lower group-channel to baseband and the center group channel, already brought to baseband by the down-converter 702, would merely be filtered to exclude the contributions from the upper and lower group channels. The decimation filter following the down-conversion of the upper group channel filters contributions from the middle and lower group channel, and the decimation filter following the down-

conversion of the lower group channel filters the contribution from the middle and upper group channels. The equivalent passband frequency at each down-converter equals the sum of all down-converter frequencies up to and including the down-converter of interest. That is, if the multiplication frequency of down converter 702 is ω_a and the multiplication frequency of down converter 704 is ω_b, the equivalent passband frequency of down-converter 704 is $(\omega_a + \omega_b)$. If the ratio of the sample rate entering a given down-converter m divided by its down-conversion frequency ω_m is an integer, then the down-converter may be constructed using a multiplier-less circuit containing a multi-position switch and CSD circuits. CSD circuits may be used to produce the decimation filters ~~702~~ 728 through ~~726~~ 752 and down-converters ~~728~~ 702 through ~~752~~726, thereby eliminating the need for costly multipliers.

Please replace paragraph beginning on page 19, line 8 with the following replacement paragraph:

The receiver 110 includes data memory 1204 for storage of input complex (inphase and quadrature, or I and Q) data sampled at least twice each channel's respective symbol rate. In an illustrative embodiment the data memory 1204 is organized as a circular buffer, so that, as data are read out of a location and used in detecting input signals, new data are written in behind the read values. The memory 1204 stores the I and Q information from all channels within a band of interest. A clock ~~1206~~ 1203 operates at twice the total symbol rate of all the channels received by the receiver and, as will be discussed in greater detail, controls the timing of the various operations within the receiver 110. The receiver 110 includes an equalizer subsystem 1206, that in turn, includes an equalizer 1208, equalizer state storage 1210, an equalizer tap matrix 1212,

and an equalizer delayline matrix 1214. The receiver 110 employs the equalizer subsystem 1206 to rid incoming signals of inter-symbol interference. Equalizers are known, and discussed, for example, in U.S. Patent 4,004,226 entitled QAM RECEIVER HAVING AUTOMATIC ADAPTIVE EQUALIZER, issued to Qureshi, et. al. (Qureshi), which is hereby incorporated by reference.

Please replace the paragraph beginning on page 19, line 23 with the following replacement paragraph:

A phase tracking subsystem 1216 includes a phase tracking loop (phase recovery) 1218 and phase tracking storage (phase state) 1220. Phase tracking loops are know and discussed, for example, in U.S. Patent 5,796,786 entitled PHASE ERROR DETECTING METHOD AND PHASE TRACKING LOOP CIRCUIT, issued to Myeoung-hwan Lee, which is hereby incorporated by reference. A time tracking subsystem 1222 includes a time tracking loop (time recovery) 1224 and time tacking storage (time state) 1226. Time tracking loops and timing recovery circuits are known and discussed, for example, in U.S. Patent 4,004,226 issued to Qureshi, and discussed above. An indexer 1228 operates to provide the time tracking phase locked loop 1224, the phase tracking phase locked loop 1218, and the equalizer 1208 with state, tap, and delayline information corresponding to the channel data being processed at a given time.

Please replace the paragraph beginning on page 20, line 4 with the following replacement paragraph:

For clarity and ease of description, we will discuss the operation of the receiver 110 in terms of a DOCSIS implementation but the receiver may find application in any mult-channel

communications system such as previously described. In operation I and Q data are written to data memory 1204, with data from each channel written to a separate section of data memory. For example, I_1 Q_1 data are written into data memory segment 1, I_2Q_2 data are written into data segment 2, I3 Q3 data are written into data memory segment 3; with, ~~I_n~~-I_N and ~~Q_n~~-Q_N data from the ~~nth~~ Nth channel written into the ~~nth~~ Nth data memory segment. Data are written into the data memory segments after older data are read out, using selector 1205, for use in one cycle, but before newer data are needed for the next cycle. This cycling may be accomplished in various ways, but, in this illustrative embodiment, the overall rate at which the data are written to the data memory (and the rate at which is written to the equalizer) is at least twice the total symbol rate of all the channels from which data are received.

Please replace the paragraph beginning on page 21, line 14 with the following replacement paragraph:

As data are simultaneously transferred into the data channel locations from a sampled data source and to the equalizer subsystem 1206 and correction loops 1218 and 1224 from the data channel locations in memory 1204, the indexer 1228 provides an indication to the equalizer subsystem 1206 the time tracking loop 1224, and the phase tracking loop 1218 of the channel associated with the data being transferred from the data memory at any given time. The indexer 1228 thereby provides to the time tracking loop 1224 the current values of the time tracking loop state and current timing estimates, to the phase tracking loop 1218 the current values of the phase tracking loop state, current equalizer output, current symbol slicer 1230 output, and current error value 1232 (which may, for example, be a least mean squared update value), and to the equalizer

1208, current tap values, current delayline values, and current phase tracking loop state values, all associated with the current sampled data values being transferred from the data memory associated with a channel that is currently being processed.

Please replace the paragraph beginning on page 21, line 27 with the following replacement paragraph:

Turning now to Figure 13, each channel can accommodate different symbol rates and, in the illustrative example of Figure 13 channels 1 through "~~n~~N" respectively operate at 1.28, .64, .32, and .32 million symbols per second and the total symbol rate of all channels, that of the group channel, is 2.56 mega-symbols per second. The maximum sample rate for the sum of the channels, twice the symbol rate, is 5.12 million samples per second. In the illustrative embodiment, there are a total of thirty two data locations within the data memory 1204, with the number of data locations devoted to a channel in proportion to the channel's data rate. For example, channel one, with a data rate twice that of channel two, and four times that of channels three and ~~n~~N, may have sixteen data locations in data memory, with eight dedicated to channel two, and four each to channels three and ~~n~~N. With data written to each channel data segment at twice the respective channel's symbol rate, each channel data segment will be "filled" in the same amount of time. And, with the output clock CLK operating at twice the group channel symbol rate, data are read out of all the data locations and written to the equalizer in a manner that does not require buffering.

Please replace the paragraph beginning on page 22, line 13 with the following replacement paragraph:

For example, in the illustrative circular buffer embodiment of Figure 13, as data from location 1 is read out and written to the equalizer, data are written into the data locations "behind" the readout. Consequently, as the output data are transferred out of channel data locations 1 through 16 to the equalizer at the output clock rate, CLK, and new data are written in behind at the rate of[[.]] CLK/2, new data are written into location 1 as old data are transferred from location 2, new data are written to location 2 as old data are transferred from location 4, ..., new data are written into location 8 as old data are transferred from location 16, new data are written into location 16 as old data are transferred from location 32, and the cycle then repeats. Similarly, other channel data locations are filled at their corresponding clock rates after older data are written to the equalizer, so that, for example, data may be written into locations 1, 17, 25, and 29 at approximately the same time data are written from location 1 into the equalizer and data may be written into locations 16, 24, 28 and 32 at approximately the same time that data are written from location 32 to the equalizer.

Please replace the paragraph beginning on page 22, line 27 with the following replacement paragraph:

In this illustrative embodiment, the indexer 1228 is an index vector having index values corresponding to the channel associated with data that is currently being transferred from data memory 1204 organized as a data vector. For example, with a data vector of thirty-two locations, the first sixteen of which are allocated to channel CH1, the next eight of which are allocated to channel CH2, the next four allocated to channel CH3, and the last four allocated to channel ~~CH4~~CHN, the first sixteen locations of the index vector include an indication of channel CH1,

the next eight locations include an indication of channel CH2, the next four include an indication of channel CH3, and the last four include an indication of channel ~~CH4~~CHN.

Please replace the paragraph beginning on page 23, line 7 with the following replacement paragraph:

As data are simultaneously transferred into the data channel locations for channels CH1 through ~~CH4~~ CHN from a sampled data source at respective rates of CLK/2, CLK/4, CLK/8, and CLK/8 and to the equalizer 1208 and time tracking loop, the index vector provides an indication to the equalizer 1208 the time tracking loop 1224, and the phase tracking loop (phase recovery) ~~1226~~ 1218 of the channel associated with the data being transferred from the data memory at any given time. As the index vector is clocked through, along with the data vector, the index vector permits the time tracking loop to select the current values of the time tracking loop state and current timing estimates by indicating the appropriate row within the time tracking loop vector ~~1220~~1226. Similarly, the index vector provides an indication to the phase tracking loop the current values of the phase tracking loop state, current equalizer output, current symbol slicer output, and current error value by pointing to the appropriate row within the phase tracking loop vector ~~1226~~1220. The index vector also provides an indication to the equalizer 1208 of current tap values, current delayline values, and current phase tracking loop state values, all associated with the current sampled data values being transferred from the data memory associated with a channel that is currently being processed by pointing to the appropriate locations within the equalizer tap matrix, the equalizer delayline matrix 1214 and phase tracking loop state vector

~~1226~~1220. The index vector may be filled at configuration with index values that reflect channel assignments through a one-to-one mapping with the entries of the input data vector 1204.

Please replace the paragraph beginning on page 23, line 26 with the following replacement paragraph:

In operation, as data is transferred from the input data vector 1204 at the CLK rate, corresponding index values, clocked out at the same rate, step the phase tracking loop, time tracking loop, and equalizer through corresponding state and other values, as previously described. Data is transferred from the input data vector 1204 to the time tracking loop and the equalizer ~~1204~~1208. State information is transferred from the time tracking loop state vector to the time tracking loop, as guided by the index vector 1228. State information is updated in the time tracking loop state vector. The time tracking loop produces a current timing error value. The "equalized" data is passed from the ~~equaiizer~~ equalizer 1208 to the phase tracking loop for phase correction and tracking. The phase tracking loop obtains state information from the phase tracking loop state vector and updates the state information. The updated state information is written back to the state vector ~~1226~~1220. The phase tracking loop produces a phase correction value which is used to rotate the equalizer output and thereby reduce phase error. The phase correction value is also used to de-rotate the equalizer update error. The de-rotated equalizer update error is written to an equalizer state vector.

Please replace the paragraph beginning on page 24, line 12 with the following replacement paragraph:

Equalizer tap values and delayline values are updated, respectively, from the equalizer tap matrix 1212 and to the equalizer delayline matrix 1214. The equalizer tap matrix and delayline matrix are sized to accommodate the delay spread of the widest upstream channel, taking into account whether a fractionally-spaced equalizer is used. In this illustrative embodiment, we assume that the equalizer 1208 is a T/2 fractionally spaced decision feedback equalizer, with eight feedforward and sixteen feedback taps. This illustrative embodiment is sized to process a single DOCSIS group channel, and as such can receive up to sixteen .2 MHz baseband channels, therefore the equalizer matrices and the phase and timing state vectors are sixteen rows deep, one row for each channel. Coefficients from a row of the tap matrix, as indicated by the index vector, are fed to the equalizer taps. Input data from the input data vector 1204 and a corresponding hard decision value ~~decision value~~ from the phase tracking state vector 1220 are respectively applied to the equalizer's feedforward delayline and feedback delayline. The equalizer multiplies the feedforward and feedback delaylines by the appropriate set of taps. The equalizer sums the results of these multiplications and the resulting preliminary symbol value is used by the phase tracking circuit to determine a phase correction for the next time cycle. A symbol slicer within the phase tracking circuit determines the nearest valid symbol to the preliminary symbol value and this value is used to update the phase tracking state vector hard decision value. Since four multiplies are required for each complex tap, the equalizer is clocked at four times the symbol rate and a single multiplier is used for each tap. The least mean squared error is updated and the tap values are written back to the tap matrix. Forward error correction (not shown) may similarly employ the index vector and state vectors for de-scrambler and Reed-Solomon decoder

algorithms. The slicer output, stored in the phase tracking loop state vector, is mapped to bits, which are then fed to a de-scrambler.